

Hindbookcenter



Hind Book Center & Photostat

MADE EASY

**Electronics Engineering
Toppers Handwritten Notes
Microprocessor
By-M.V.R Shastri Sir**

- Colour Print Out
- Blackinwhite Print Out
- Spiral Binding,& Hard Binding
- Test Paper For IES GATE PSUs IAS, CAT,SSC
- All Notes Available & All Book Availabile
- Best Quaity Handwritten Classroom Notes & Study Materials
- IES GATE PSUs IAS CAT Other Competitive/Entrence Exams

Visit us:-www.hindbookcenter.com

**Courier Facility All Over India
(DTDC & INDIA POST)
Mob-9711475393**



Hindbookcenter



ALL NOTES BOOKS AVAILABLE ALL STUDY MATERIAL AVAILABLE
COURIERS SERVICE AVAILABLE

MADE EASY, IES MASTER, ACE ACADEMY, KREATRYX

ESE, GATE, PSUs BEST QUALITY TOPPER HAND WRITTEN NOTES
MINIMUM PRICE AVAILABLE @ OUR WEBSITE

- | | |
|--------------------------------|---------------------------|
| 1. ELECTRONICS ENGINEERING | 2. ELECTRICAL ENGINEERING |
| 3. MECHANICAL ENGINEERING | 4. CIVIL ENGINEERING |
| 5. INSTRUMENTATION ENGINEERING | 6. COMPUTER SCIENCE |

IES, GATE, PSU TEST SERIES AVAILABLE @ OUR WEBSITE

- ❖ IES –PRELIMS & MAINS
- ❖ GATE

➤ NOTE;- ALL ENGINEERING BRANCHS

➤ ALL PSUs PREVIOUS YEAR QUESTION PAPER @ OUR WEBSITE

PUBLICATIONS BOOKS -

MADE EASY, IES MASTER, ACE ACADEMY, KREATRYX, GATE ACADEMY, ARIHANT, GK
RAKESH YADAV, KD CAMPUS, FOUNDATION, MC –GRAW HILL (TMH), PEARSON...OTHERS

HEAVY DISCOUNTS BOOKS AVAILABLE @ OUR WEBSITE

| | | | |
|--|---|--|--|
| Shop No.7/8 Saidulajab Market Neb Sarai More, Saket, New Delhi-30 | Shop No: 46 100 Futa M.G. Rd Near Made Easy Ghitorni, New Delhi-30 | F518 Near Kali Maa Mandir Lado Sarai New Delhi-110030 | Shop No.7/8 Saidulajab Market Neb Sarai More, Saket, New Delhi-30 |
|--|---|--|--|

Website: www.hindbookcenter.com

Contact Us: 9711475393

MICROPROCESSOR:

- i) 8085. (Gate - in detail) ———→ 2M/3M GATE
- ii) 8086.
- iii) 8051.

Note:.

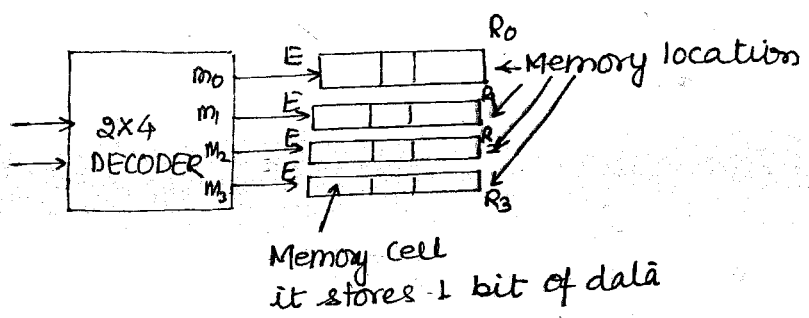
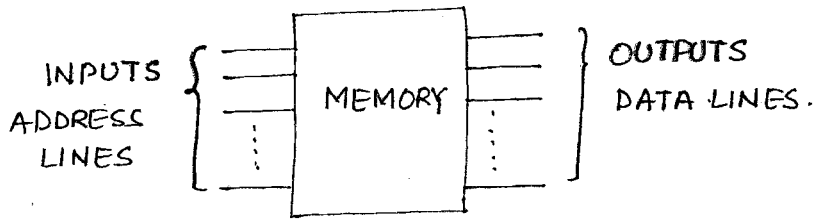
** IAS/IPS
 ELECTRICAL OPTIONAL
 (MAINS)
 ↓
 ECE + EEE
 ** BEFORE 2011
 IAS PRELIMS ELECTRICAL
 GATE STANDARD
 (OBJECTIVE).

8085 SYLLABUS:

- i) Memories.
 - ii) 8085 Basics.
 - iii) Instruction set
 - iv) Programming
 - v) Interfacing
- } 1 MARKS GATE
- } ** 2 MARKS GATE

* MEMORIES:

* Used for storage.



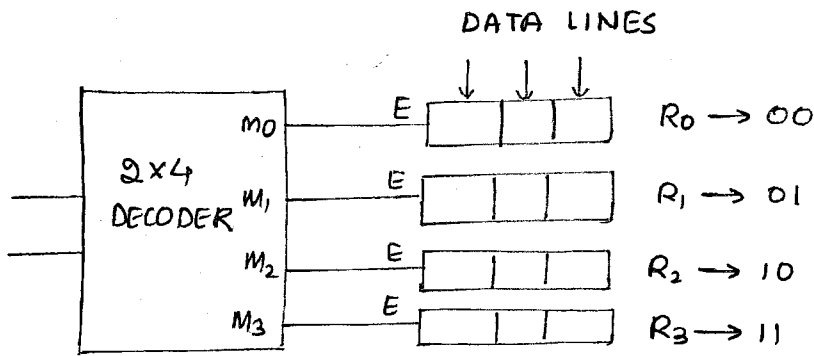
Note:.

- * By giving input 00, m₀ will get selected hence the address of R₀ is 00.
- * By giving input 01, m₁ will get selected hence the address of R₁ is 01.

| MEMORY LOCATION | ADDRESS |
|-----------------|---------|
| R ₀ | 00 |
| R ₁ | 01 |
| R ₂ | 10 |
| R ₃ | 11 |

* ADDRESS:

* ADDRESS is a binary code which enables a particular location



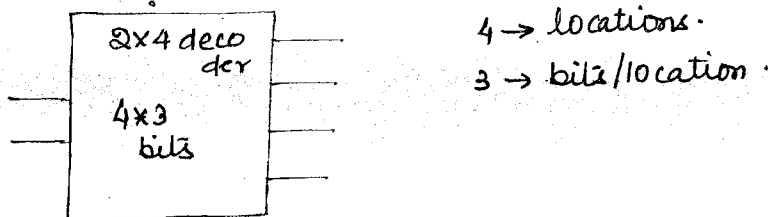
* In order to store data in memory the following sequence has to be followed:

- i) Select the location by giving an appropriate address.
- ii) Give the data through the Data lines.

* SIZE OF

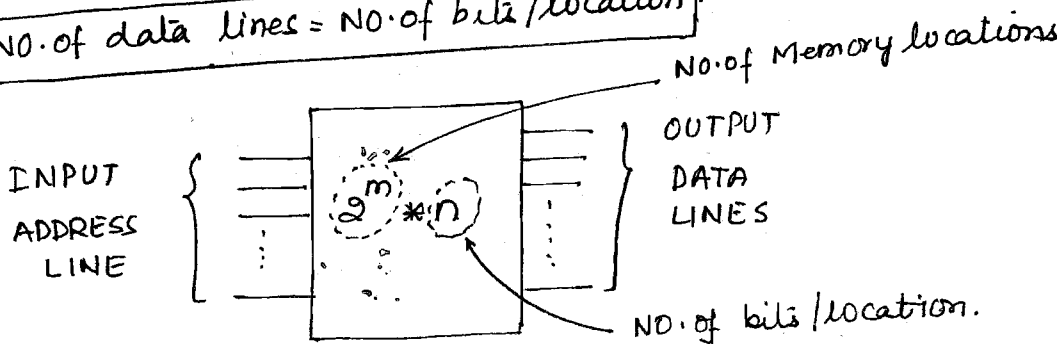
* Size of Memory is measured in bits and is equal to NO. of memory location multiplied with NO. of bits/location

$$\text{Memory Size} = \text{NO. of memory location} \times \text{NO. of bits/location}$$

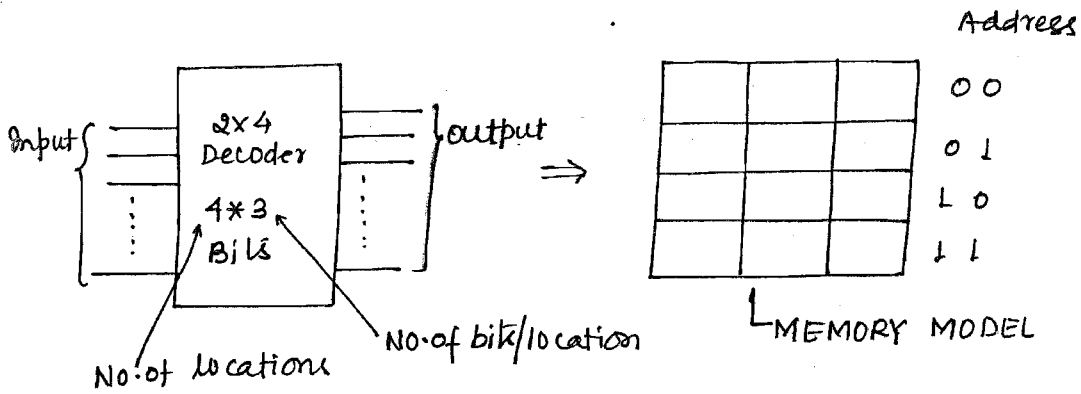


* For m address lines, no. of location is 2^m .

* $\text{NO. of data lines} = \text{NO. of bits/location}$



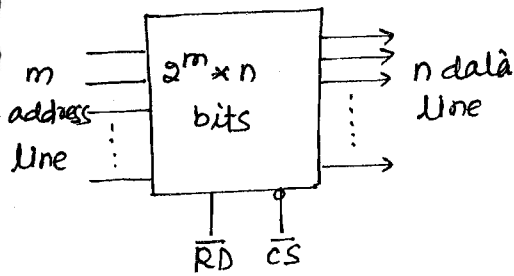
* MODEL OF MEMORY:



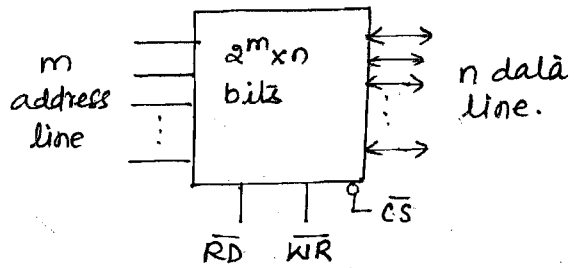
* Two types of Memory:

- i) Read only Memory (ROM)
- ii) Read/write Memory (RWIM)
 ↳ commercially called RAM.

READ ONLY MEMORY:



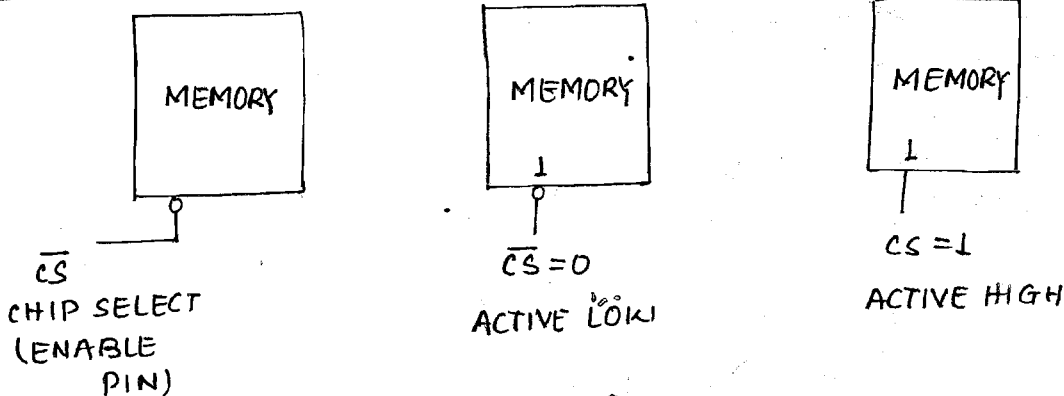
RANDOM ACCESS MEMORY



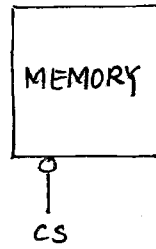
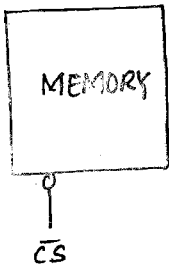
* Unidirectional data line to only Read data.

* Bidirectional data line to Read and write data

Note:



MOST CORRECT



*NOTE!

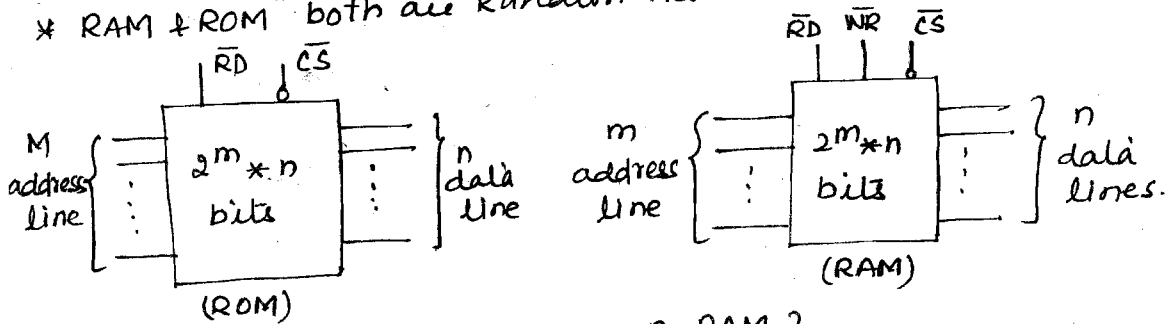
*All are 3 possible ways of Representing CHIP SELECT.

*RAM

*Random Access v/s Serial Access!

*In Random access we directly give the address and reach the location where data is stored, but in Serial access to reach some location we have to go serially

*RAM & ROM both are Random Access.



Q1) Construct 8KB RAM using 2KB RAM?

Soln: Kilo $\rightarrow 2^{10}$ Bits ; Mega $\rightarrow 2^{20}$ Bits ; Giga $\rightarrow 2^{30}$ Bits.

* Requirement is 8KB

B: Bytes

8 bits make a Byte

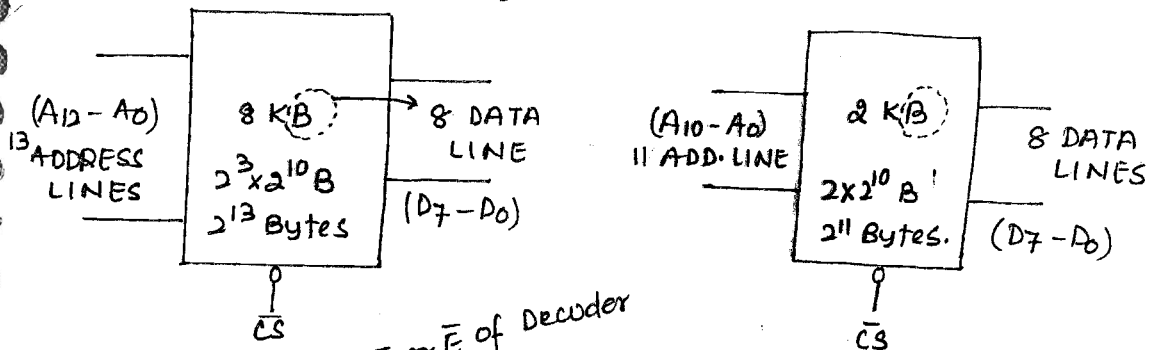
memory location \rightarrow (8K) B \leftarrow 8 bits/location

$$8K \rightarrow 2^3 \times 2^{10} = 2^{13} = 2^m$$

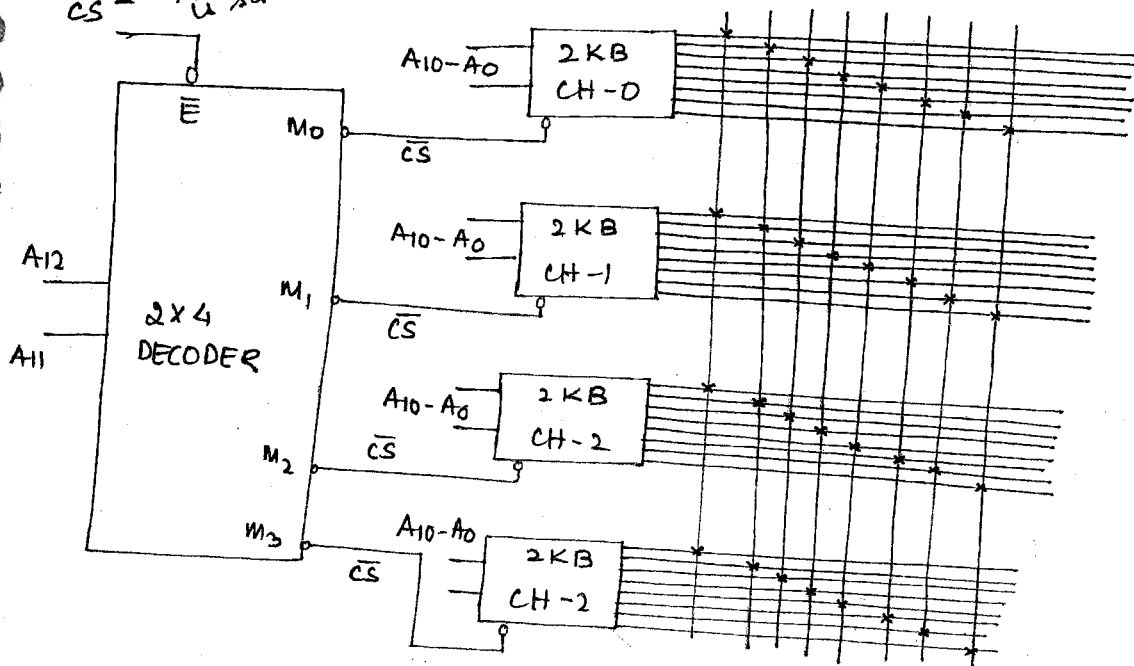
$m=13$ \leftarrow Address lines.

data lines = 8

B → Bytes i.e 8 bit



CS ← of 8 KB RAM is same as CS or \bar{E} of Decoder



Note!:

| | | 2 KB RAM | | | | | | | | | | |
|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| A ₁₂ | A ₁₁ | A ₁₀ | A ₉ | A ₈ | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ |
| 0 | 0 | CHIP 0 | | | | | | | | | | |
| 0 | 1 | CHIP 1 | | | | | | | | | | |
| 1 | 0 | CHIP 2 | | | | | | | | | | |
| 1 | 1 | CHIP 3 | | | | | | | | | | |

Q2) construct 32 KB ROM using 4 KB ROM.

Soln. 32 KB ROM

$2^5 \times 2^{10}$ Bytes

Address lines = 15

Data line = 8

4 KB ROM

$2^2 \times 2^{10}$ Bytes

Address line = 12.

Data line = 8.

~~A13~~
A14
A13
A12

